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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,629	YADA ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/27/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Objections

2. Claim 25 is objected to because of the following informalities: In line 4 of claim 25, "the CPU is capable of storing" is incorrect. It should be --the CPU stores--. Appropriate correction is required.

3. Claim 32 is objected to because of the following informalities: In line 3 of claim 32, "memory capable of storing" is incorrect. It should be --memory stores--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-2, 5, 15, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021) in view of Weng et al. (US 5,428,630).

As per claim 1, Saito et al. teach a data processing system (col. 2, line 21, Saito et al.) comprising: an erasable and programmable non-volatile memory (col. 4, line 31, Saito et al.); a central processing unit (col. 5, line 11, Saito et al.) and a specified partial storage area of the non-volatile memory and other storage areas of the non-volatile memory (col. 2, lines 21-25, Saito et al.).

However Saito et al. do not explicitly teach the specific use of the central processing unit executing a predetermined process to thereby carry out a process for increasing the number of assurances for rewriting in a storage area.

Weng et al. in an analogous art teach that error correcting code (ECC) strategies are used to recover data that may have been corrupted. When a data block is to be written to the mass memory medium, the DMA control logic initially stores the data block in the local memory. The data block is stored in the local memory as a sequence of data symbols. The DMA control logic then retrieves the data block, which is then provided to the ECC encoder. The ECC encoder encodes the retrieved data block with error correction data. The error correction data comprises a sequence of error correction symbols that are appended to the data symbols. The DMA logic then instructs the mass memory control logic to store the data and error correction symbols in the mass memory (col. 1, lines 18-20, lines 60-68, col. 2, lines 1-3, Weng et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Weng et al. by including an additional step of the central processing unit executing a predetermined process to thereby carry out a process for increasing the number of assurances for rewriting in a storage area.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect errors in the data stored and recover the data.

- As per claim 2, Saito et al. and Weng et al. teach the additional limitations.

Saito et al. teach a data processing system (col. 2, line 21, Saito et al.) comprising: an erasable and programmable non-volatile memory (col. 4, line 31, Saito et al.); and a central processing unit (col. 5, line

11, Saito et al.) and a specified partial storage area of the non-volatile memory (col. 2, lines 21-25, Saito et al.).

Weng et al. teach executing a predetermined process to thereby generate error correcting information and add the same to data to be written in and allow an error decision and an error correction based on the error correcting information to be effected on the data read (col. 1, lines 60-68, col. 2, lines 1-22, Weng et al.).

- As per claim 5, Saito et al. and Weng et al. teach the additional limitations.

Saito et al. teach partial storage area of the non-volatile memory (col. 2, lines 21-25, Saito et al.).

Weng et al. teach that the predetermined process comprises an error-correcting information generating program for generating error correcting information for the data written, and an error-correcting program for effecting an error decision and an error correction on data with error correcting information read (col. 1, lines 60-68, col. 2, lines 1-22, Weng et al.).

- As per claim 15, Saito et al. and Weng et al. teach the additional limitations.

Weng et al. teach the data processing system, wherein the central processing unit has means for holding information indicative of the occurrence of an error uncorrectable in the error determining process under the execution of the error-correcting program, recognizably from the outside (figure 3, col. 2, lines 10-22, Weng et al.).

- As per claim 16, Saito et al. and Weng et al. teach the additional limitations.

Saito et al. teach a data processing system comprising: a first storage area low in the number of rewrite assurances; and a second storage area high in the number of rewrite assurances, both being provided in an address space of an arithmetic control device (col. 2, lines 21-25, lines 39-43, col. 3, lines 45-46, Saito et al.).

Weng et al. teach an ECC code generating for generating each of ECC codes for data and an error correcting for effecting an error decision and an error correction on data with the ECC codes read, and the arithmetic control device executes the ECC code generating (figure 3, col. 1, lines 60-68, col. 2, lines 1-22, Weng et al.).

- As per claim 17, Saito et al. and Weng et al. teach the additional limitations.

Saito et al. teach the second storage area (col. 2, lines 21-25, Saito et al.). Weng et al. teach that the arithmetic control device executes the error-correcting program (figure 3, col. 7, lines 51-55, Saito et al.).

7. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021) and Weng et al. (US 5,428,630) as applied to claim 2 above, and further in view of Yamauchi (US 5,097,445).

As per claim 3, Saito et al. and Weng et al. substantially teach the claimed invention described in claim 2 (as rejected above).

However Saito et al. and Weng et al. do not explicitly teach the specific use of the data processing system, which is a single chip type microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip.

Yamauchi in an analogous art teaches the semiconductor integrated circuit, wherein the non-volatile memory capable of rewriting is an EEPROM, said CPU and peripheral circuit thereof have a CMOS structure, and said EEPROM is a MNOS structure, and all these circuits are mounted on a single silicon chip (figure 5, col. 9, lines 27-32, Yamauchi).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Yamauchi by including an additional step of using the data processing system, which is a single chip type microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to increase processing speed of memory data by the CPU and reduce the additional circuit cost.

- As per claim 4, Saito et al., Weng et al. and Yamauchi teach the additional limitations.

Yamauchi teaches the data processing system, which is configured in a multi-chip form wherein the non-volatile memory and the central processing unit are respectively formed on discrete semiconductor chips (EEPROM 41 and external CPU 1 in figure 1, Yamauchi).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021) and Weng et al. (US 5,428,630) as applied to claim 5 above, and further in view of Woffinden et al. (US 4,780,809).

As per claim 6, Saito et al. and Weng et al. substantially teach the claimed invention described in claim 5 (as rejected above).

However Saito et al. and Weng et al. do not explicitly teach the specific use the data processing system, which has a storage area for a matrix table wherein when the data is configured as n bits and error correcting information for the n-bit data is defined as m bits, mutually-different binary numbers of m bits are arranged in an m+n array, and wherein the matrix table is referred to the error-correcting information generating program and the error-correcting program.

Woffinden et al. in an analogous art teach that mainstore ECC logic consists of an 8-bit Hamming code described by the Hamming matrix 'H' shown in Table 1. This code is generated by the mainstore move-in ECC code generator 12-4 with .....signal an error condition 12-74 (table 1, col. 6, lines 64-66, col. 7, line 43 – col. 8, line 44, Woffinden et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Woffinden et al. by including an additional step of using the data processing system, which has a storage area for a matrix table wherein when the data is configured as n bits and error correcting information for the n-bit data is defined as m bits, mutually-different binary numbers of m bits are arranged in an m+n array, and wherein the matrix table is referred to the error-correcting information generating program and the error-correcting program.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to check the error and correct the error when the data stored in the memory is retrieved.

9. Claims 7, 19, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021) and Weng et al. (US 5,428,630) as applied to claim 5 above, and further in view of Okugaki et al. (US 5,450,424).

As per claim 7, Saito et al. and Weng et al. substantially teach the claimed invention described in claim 5 (as rejected above).

However Saito et al. and Weng et al. do not explicitly teach the specific use the data processing system, further including a mask ROM accessible by the central processing unit, and wherein the mask ROM has the error-correcting information generating program and the error-correcting program.

Okugaki et al. in an analogous art teach that FIG. 14 schematically illustrates the overall structure of a general mask ROM that is provided with an ECC function (figure 14, col. 2, lines 64-66, Okugaki et al.). Okugaki et al. also teach that the mask ROM further includes an ECC circuit 614 for checking errors with respect to the data (the information bits and the error checking bit), (col. 3, lines 25-27, Okugaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Okugaki et al. by including an additional step of using the data processing system, further including a mask ROM accessible by the central processing unit, and wherein the mask ROM has the error-correcting information generating program and the error-correcting program.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to check and correct an error in the information bits that are stored in the memory.

- As per claim 19, Saito et al., Weng et al. and Okugaki et al. teach the additional limitations.

Okugaki et al. teach that the first storage area is a mask ROM (figure 14, col. 2, lines 64-66, Okugaki et al.).

Saito et al. teach that the second storage area is an electrically erasable and programmable flash memory (col. 4, line 31, Saito et al.).

- As per claim 23, Saito et al., Weng et al. and Okugaki et al. teach the additional limitations.

Okugaki et al. teach the data processing system, wherein the central processing unit has a storage circuit for holding, when error-correctable data is detected during the execution of the error-correcting program, information corresponding to the result of detection (figure 14, col. 3, lines 25-31, lines 34-38, lines 51-55, Okugaki et al.).

- As per claim 24, Saito et al., Weng et al. and Okugaki et al. teach the additional limitations.

Okugaki et al. teach the data processing system, wherein the information corresponding to the result of detection is used as warning information (col. 3, lines 44-47, Okugaki et al.).

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021) and Weng et al. (US 5,428,630) as applied to claim 5 above, and further in view of Okamoto et al. (US 4,677,622).

As per claim 8, Saito et al. and Weng et al. substantially teach the claimed invention described in claim 5 (as rejected above).

However Saito et al. and Weng et al. do not explicitly teach the specific use the data processing system, wherein the other storage areas of the non-volatile memory have areas for storing the error-correcting information generating program and the error-correcting program.

Okamoto et al. in an analogous art teach program memory means for storing a program for controlling said arithmetic logic circuit means and said data memory means so as to perform the error correcting operation and addition of flags (col. 22, lines 32-35, Okamoto et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Okamoto et al. by including an additional step of using the data processing system, wherein the other storage areas of the non-volatile memory have areas for storing the error-correcting information generating program and the error-correcting program. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to execute the error correcting program by the CPU to generate error-correcting information and correct the errors in the information bits that are stored in the memory.

11. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021), Weng et al. (US 5,428,630) and Okamoto et al. (US 4,677,622) as applied to claim 8 above, and further in view of Uekubo et al. (US 6,198,657 B1).

As per claim 9, Saito et al., Weng et al. and Okamoto et al. substantially teach the claimed invention described in claim 8 (as rejected above).

Okamoto et al. teach the areas for storing the error-correcting information generating program and the error-correcting program (col. 22, lines 32-35, Okamoto et al.).

However Saito et al., Weng et al. and Okamoto et al. do not explicitly teach the specific use the data processing system, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed.

Uekubo et al. in an analogous art teach that the erasure prohibiting circuit of the present invention may be provided such that erasure of the entire area of the memory cell array is prohibited, or such that erasure of a part of the memory cell is prohibited by combination with address signals.

A nonvolatile memory device provided with an erasure prohibiting circuit for prohibiting erasure of the content of data in said nonvolatile memory device, wherein said erasure prohibiting circuit permanently prohibits erasure of the data when an instruction to prohibit erasure is directed from the outside of said nonvolatile memory device.

A nonvolatile memory device, wherein said erasure prohibiting circuit comprises an erasure prohibiting memory portion for storing either one of first information for prohibiting erasure or second information for permitting erasure (col. 17, lines 8-12, lines 44-54, Uekubo et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Uekubo et al. by including an additional step of using the data processing system, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to separate the area of the memory for erase and writing allowable and non-allowable areas and to increase the reliability of information storage in the memory.

- As per claim 10, Saito et al., Weng et al., Okamoto et al. and Uekubo et al. teach the additional limitations.

Saito et al. teach partial storage area (col. 2, lines 21-25, Saito et al.).

Weng et al. teach the data processing system, wherein the error-correcting information generating program serves so as to generate error correcting information and thereafter store the generated error correcting information and data corresponding thereto in accordance with a prescribed format as data with the error correcting information, and the error-correcting program serves so as to recognize the data with the error correcting information in accordance with the prescribed format (col. 1, lines 60-68, col. 2, lines 1-22, Weng et al.).

- As per claim 11, Saito et al., Weng et al., Okamoto et al. and Uekubo et al. teach the additional limitations.

Okamoto et al. teach the areas for storing the error-correcting information generating program and the error-correcting program (col. 22, lines 32-35, Okamoto et al.).

Uekubo et al. teach the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed (col. 17, lines 8-12, lines 44-54, Uekubo et al.).

12. Claims 12, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021) and Weng et al. (US 5,428,630) as applied to claim 5 and claim 16 above respectively, and further in view of Yoshimura (US 6,546,517 B1).

As per claim 12, Saito et al. and Weng et al. substantially teach the claimed invention described in claim 5 (as rejected above). Weng et al. teach the error-correcting information generating and the error-correcting (col. 1, lines 60-68, col. 2, lines 1-22, Weng et al.).

However Saito et al. and Weng et al. do not explicitly teach the specific use the data processing system, further including a RAM to which program are transferred from the non-volatile memory, and wherein the central processing unit executes the program transferred to the RAM.

Yoshimura in an analogous art teaches that the RAM 2 includes a first storage region 91 serving as a dynamic load area to which a program code stored in each of the blocks of the flash memory group 4 is exclusively loaded. Such program code transfer from the flash memory group 4 to the RAM 2 is executed,

e.g., by the CPU 1 based on a program previously stored in the ROM 3 (figure 1-2, col. 3, lines 31-36, Yoshimura).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Yoshimura by including an additional step of using the data processing system, further including a RAM to which program are transferred from the non-volatile memory, and wherein the central processing unit executes the program transferred to the RAM.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to execute the specific program stored in the non-volatile memory for specific function and process the data fast and accurately.

- As per claim 18, Saito et al., Weng et al. and Yoshimura teach the additional limitations.

Yoshimura teaches sequentially transferring the data of the second storage area to the RAM in advance (figure 1-2, col. 3, lines 31-36, Yoshimura).

Weng et al. teaches that the arithmetic control device is capable of executing the error-correcting program in response to a predetermined operation mode (col. 2, lines 4-22, Weng et al.).

- As per claim 20, Saito et al., Weng et al. and Yoshimura teach the additional limitations.

Yoshimura teaches that each of the first storage area and the second storage area is an electrically erasable and programmable flash memory, the flash memory has a write/erase program for the flash memory, and further including a RAM to which the write/erase program is transferred from the flash memory, and wherein the arithmetic control device is capable of executing the write/erase program placed on the RAM in response to a specific operation mode (figure 1-2, col. 3, lines 31-36, Yoshimura).

13. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (US 6,000,021), Weng et al. (US 5,428,630) and Yoshimura (US 6,546,517 B1) as applied to claim 12 above, and further in view of Fudeyasu et al. (JP 11219299 A).

As per claim 13, Saito et al., Weng et al. and Yoshimura substantially teach the claimed invention described in claim 12 (as rejected above).

Weng et al. teach the error-correcting information generating and the error-correcting (col. 1, lines 60-68, col. 2, lines 1-22, Weng et al.).

However Saito et al., Weng et al. and Yoshimura do not explicitly teach the specific use of the data processing system, wherein the central processing unit transfers the program from the non-volatile memory to the RAM in response to reset instructions.

Fudeyasu et al. in an analogous art teach that in a boot mode for transferring the boot program for transferring the E/W program for rewriting the data of the flash ROM 3 from the outside to the RAM, from a boot ROM 4 to the RAM 2 and reading and executing the boot program transferred to the RAM 2 from a CPU 1, by arranging a reset interruption vector inside the boot ROM 4 and all the other interruption vectors inside the RAM 2 respectively, the execution of the interruption processing from the E/W program transferred to the RAM 2 is made possible (abstract, Fudeyasu et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Saito et al.'s patent with the teachings of Fudeyasu et al. by including an additional step of using the data processing system, wherein the central processing unit transfers the program from the non-volatile memory to the RAM in response to reset instructions.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to execute the program to perform specific tasks such as error checking and correcting when reset occurs.

- As per claim 14, Saito et al., Weng et al., Yoshimura and Fudeyasu et al. teach the additional limitations.

Yoshimura teach a RAM accessible by the central processing unit and storing the data in the RAM (figure 1-2, col. 3, lines 31-36, Yoshimura).

Saito et al. teach the partial storage area of the non-volatile memory (col. 2, lines 21-25, Saito et al.).

Fudeyasu et al. teach reading data in response to reset instructions (abstract, Fudeyasu et al.).

Weng et al. teach reading data with error correcting information and affecting the error decision and error correction on the read data with error correcting information according to the execution of the error-correcting program (col. 1, lines 60-68, col. 2, lines 1-22, Weng et al.)

14. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woffinden et al. (US 4,780,809) in view of Ebihara et al. (US 6,219,807 B1).

As per claim 21, Woffinden et al. teach a data processing method using a matrix table wherein when ECC codes are defined as m bits with respect to data of n bits, mutually-different binary numbers of m bits are arranged in an m+n array (table 1, col. 6, lines 64-66, col. 7, lines 43-49, Woffinden et al.).

However Woffinden et al. do not explicitly teach the specific use of exclusive-ORing values in columns of the matrix table, corresponding to bit positions of logical values "1" of data every bits as viewed in a row direction upon generating the ECC codes; setting the values of m bits obtained from the exclusive-ORing as the ECC codes; and adding the ECC codes to data respectively to thereby generate code words of m+n bits.

Ebihara et al. in an analogous art teach that the ECC code generation circuit of the embodiment generates the ECC code of six bits O0 to O5 whereof each has XOR logic of each different combination of 15 (odd number) bits selected from input data of 32 bits D00 to D31, such as illustrated in FIG. 1 (figure 1, col. 4, lines 20-24, Ebihara et al.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Woffinden et al.'s patent with the teachings of Ebihara et al. by including an additional step of exclusive-ORing values in columns of the matrix table, corresponding to bit positions of logical values "1" of data every bits as viewed in a row direction upon generating the ECC codes; setting the values of m bits obtained from the exclusive-ORing as the ECC codes; and adding the ECC codes to data respectively to thereby generate code words of m+n bits.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to generate error correction code that can be used to detect errors and correct the errors in the data stored.

15. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woffinden et al. (US 4,780,809) and Ebihara et al. (US 6,219,807 B1) as applied to claim 21 above, and further in view of Horiguchi et al. (US 4,726,021).

As per claim 22, Woffinden et al. and Ebihara et al. substantially teach the claimed invention described in claim 21 (as rejected above).

However Woffinden et al. and Ebihara et al. do not explicitly teach the specific use of the data processing method, further comprising exclusive-ORing values in columns of the matrix table, corresponding to bit positions of logical values "1" of the code words every bits as viewed in the row direction, making an error-free decision when the values of m bits obtained by the exclusive-ORing are of a logical value "0" in all bits to thereby set the n-bit data of the cord words as normal data, determining that an error exists when the values of m bits obtained by the exclusive-ORing are of a logical value "1" even one bit, retrieving a column coincident with a binary number of m bits obtained by the exclusive-ORing from the columns of the matrix table, inverting bits of code words at positions associated with the retrieved column in logical value and correcting the same, and defining the n-bit data of the corrected code words as normal data.

Horiguchi et al. in an analogous art teach that the construction and operation of the circuits 110 to 140 composing the error correcting function using an ECC will be described with reference to FIGS. 11 to 14.

To perform an error correcting operation using an ECC, the decoding circuit 110 is constructed of, as shown in FIG. 11, a syndrome generator 111, error location indicator 112, error correcting Exclusive-OR gate array and AND gate array. The syndrome generator 111 generates a syndrome of data X.sub.0 to X.sub.n-1 from the common I/O lines to send it to the error location indicator 112. The error location indicator 112 analyzes the syndrome to assume the error location of data X.sub.0 to X.sub.n-1, and changes only the error-assumed output line among n output lines to a logic "1" (the other lines are all made logic "0").

In this case, if an error correcting operation is to be conducted, the n outputs are directly sent to the EOR gate array via the AND gate array, so that only the error-assumed bit among data X.sub.0 to X.sub.n-1 is inverted to obtain an output Y.sub.0 to Y.sub.n-1 (figure 11-14, col. 7, lines 23-43, Horiguchi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Woffinden et al.'s patent with the teachings of Horiguchi et al. by including an additional step of using the data processing method, further comprising exclusive-ORing values in columns of the matrix table, corresponding to bit positions of logical values "1" of the code words every bits as viewed in the row direction, making an error-free decision when the values of m bits obtained by the exclusive-ORing are of a logical value "0" in all bits to thereby set the n-bit data of the cord words as normal data, determining that an error exists when the values of m bits obtained by the exclusive-ORing are of a logical value "1" even one bit, retrieving a column coincident with a binary number of m bits obtained by the exclusive-ORing from the columns of the matrix table, inverting bits of code words at positions associated with the retrieved column in logical value and correcting the same, and defining the n-bit data of the corrected code words as normal data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if the data stored in the memory is error free and if an error is found in the stored data, correct the error.

16. Claims 25-31, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi (US 5,097,445) in view of Teshigawara (JP 05046494 A) and Saito et al. (US 6,000,021).

As per claim 25, Yamauchi teaches a semiconductor integrated circuit comprising: a CPU; and an erasable and programmable non-volatile memory (figure 5, col. 1, lines 9-11, col. 6, lines 42-46, col. 9, lines 27-29, Yamauchi).

However Yamauchi does not explicitly teach specifically that the CPU is capable of storing one data in memory cells at different addresses, reading data from the memory cells at the different addresses and performing a logical operation on the read plural data to thereby effect a necessary error correction to the data.

Teshigawara in an analogous art teaches an information processing system reading and writing data in a non-volatile memory 2 is provided with a write step writing the same data on the different addresses of the nonvolatile memory 2 and a read step successively reading data written in the different addresses of

the nonvolatile memory 2 in this write step. It is also provided with a data check step comparing a plurality of data successively read out by the read step each other and outputting one of them as read data. Thus, the authenticity of data read out from the nonvolatile memory 2 is checked, resulting in reading reliable data (figure 1, 2, abstract, Teshigawara).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamauchi's patent with the teachings of Teshigawara by including additionally that the CPU is capable of storing one data in memory cells at different addresses, reading data from the memory cells at the different addresses and performing a logical operation on the read plural data to thereby effect a necessary error correction to the data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to read reliable data by checking the authenticity of data read out from a nonvolatile memory.

Yamauchi also does not explicitly teach that information is written in a specific block corresponding to part of a storage area in the non-volatile memory.

However Saito et al. in an analogous art teach that a data storage system typically includes a storage medium divided into storage areas, and multiple read/write probes each of which performs access operations to read and write data in a respective storage area of the storage medium (col. 2, lines 21-25, Saito et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamauchi's patent with the teachings of Saito et al. by including additionally that information is written in a specific block corresponding to part of a storage area in the non-volatile memory.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify the useful life of different areas of the storage medium for data storage.

- As per claim 26, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Teshigawara teaches that the number of the different addresses is two or more (figure 2, paragraph 9, detailed description, Teshigawara) and the execution of an instruction included in an instruction set of the CPU (figure 3, paragraph 10, detailed description, Teshigawara).

Yamauchi teaches that the logical operation is a logical OR operation (OR gate 43e in figure 6, col. 7, line 12, Yamauchi).

- As per claim 27, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Teshigawara teaches that the number of the different addresses is two or more (figure 2, paragraph 9, detailed description, Teshigawara), and the execution of an instruction included in an instruction set of the CPU (figure 3, paragraph 10, detailed description, Teshigawara).

Yamauchi teaches that the logical operation is a logical AND operation (AND gates 43f in figure 6, col. 7, lines 17-18, Yamauchi).

- As per claim 28, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Teshigawara teaches that the number of the different addresses is three or more, and the logical operation is an operation for effecting majority decision on the plural data read from the memory cells at the different addresses (figure 3-4, paragraph 9, 10, 11, detailed description, Teshigawara).

- As per claim 29, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Saito et al. teaches that the non-volatile memory has an area different from the specific block (col. 2, lines 21-25, Saito et al.). Teshigawara teaches a program area for storing a program executed by the CPU (figure 1-2, paragraph 8-9, detailed description, Teshigawara).

- As per claim 30, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Teshigawara teaches that the program area includes a program for storing the one data in the memory cells at the different addresses, a program for performing the error correction, and other programs (figure 1-2, paragraph 6-9, Teshigawara).

- As per claim 31, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Saito et al. teach the specific block has a product spec for assuring the number of rewritings greater than other blocks (col. 2, lines 39-43, Saito et al.).

- As per claim 33, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Yamauchi teaches the CPU and the non-volatile memory are formed on a single semiconductor chip, which constitutes a microcomputer (figure 5, col. 6, lines 42-46, Yamauchi).

- As per claim 34, Yamauchi, Teshigawara and Saito et al. teach the additional limitations.

Yamauchi teaches that the CPU and the non-volatile memory are respectively formed on separate semiconductor chips. (EEPROM 41 and external CPU 1 in figure 1, Yamauchi).

17. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi (US 5,097,445), Teshigawara (JP 05046494 A) and Saito et al. (US 6,000,021) as applied to claim 25 above, and further in view of Derhacobian et al. (US 5,991,202).

As per claim 32, Yamauchi, Teshigawara and Saito et al. substantially teach the claimed invention described in claim 25 (as rejected above).

However Yamauchi, Teshigawara and Saito et al. do not explicitly teach the specifically that the non-volatile memory is a flash memory capable of storing information therein according to high and low levels of a threshold voltage of each memory cell.

Derhacobian et al. in an analogous art teach that the inventive method is applicable to current single-level NAND flash memory systems, which operate using two threshold voltage levels per cell (e.g., "high" +1 volt or "low" -2 volts) to store one bit of information per cell (col. 5, lines 50-53, Derhacobian et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamauchi's patent with the teachings of Derhacobian et al. by including additionally that the non-volatile memory is a flash memory capable of storing information therein according to high and low levels of a threshold voltage of each memory cell.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce program disturb and reduce the time required for programming the memory.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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